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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/648,540	08/28/2000	Alexander D. Schapira	CA7010652001	7789

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EXAMINER	
GUILL, RUSSELL L	
ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
10/20/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/648,540	SCHAPIRA ET AL.	
	Examiner	Art Unit	
	Russ Guill	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,8,13-16,19-20* is/are allowed.

6)☒ Claim(s) *5-7,9-12,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an Amendment filed August 21, 2008. Claims 1 - 20 are pending. Claims 1 - 20 have been examined. Claim 5 - 7, 9 - 12 and 17 - 18 are rejected. Claims 1 - 20 are allowable over the prior art of record.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 21, 2008, has been entered.

Response to Remarks

3. As an initial issue, the Examiner remarks that a telephone interview may be useful to resolve the rejections, and review proposed claims and arguments in order to expedite the examination process.

4. Initially, in order to focus attention on the primary issue, the Examiner respectfully remarks that the primary issue regarding claims 5 and 9 is that the specification appears to require *all* of the digital outputs be in a high impedance state, rather than *at least one*, as recited in the claims, in order for the analog circuit to provide the output signal at the node.

5. Regarding **claims 5 - 7 and 9 - 12** rejected under 35 USC § 112, first paragraph:

   a. Applicant's arguments have been fully considered, but are not fully persuasive, as discussed below.

b. The Applicant argues:

c. Applicants respectfully submit that the standard for determining whether the specification meets the enablement requirement is whether "the experimentation needed to practice the invention undue or unreasonable". MPEP § 2164.01 citing Mineral Separation v. Hyde, 242 U.S. 261, 270 (1916), MPEP further mandates that "even though the statute does not use the term 'undue experimentation', it has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation." MPEP § 2164.01 citing In re Wands, 858 F.2d at 737, 8 LiSPQ2d at 141.4 (Fed. Cir. 1988).

d. In addition, Applicants respectfully submit that MPEP 2164.01(a) explicitly mandates that lilt is improper to conclude that a disclosure is not enabling based on an **analysis of only one of the above factors while ignoring one or more** of the **others."** The same section of MPEP further lists the eight factors that the Court of Appeals for the Federal Circuit requires in determining whether any necessary experimentation is undue. These factors include (A) the breadth of the claims; (B) the nature of the invention; (C) the state of the prior art, (D) the level of one of ordinary skill; (E) the level of predictability in the art; (F) the amount of direction provided by the inventor; (G) the existence of working examples; and (H) the quantity of experimentation needed to make or use the invention based on the content of the disclosure.

e. Applicants respectfully submit that the final Office action did not analyze any of the above eight factors but just summarily concluded that 'the claim(s) contains subject matter which was not described in the Specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and or use the invention." The final Office action then concludes that [o]ne reasonably skilled in the art could not make or use the invention from the disclosure int eh specification, coupled with information known in the art, without undue experimentation." Although the final Office action provides some reasons by citing to some passages in the Application,

Applicants respectfully submit that these passages merely represent one or sonic embodiments: of the invention and shall not be read into the claims to limit the scope of the claims. Applicants further respectfully submit that although the final Office action provides some reasons for the rejections under 35 U.S.C. § 112, first paragraph, which Applicants respectfully traverse, the final Office action **fails to consider the eight factors required by the** Federal Circuit **and MPEP.**

f. Therefore, Applicants respectfully submit that the ground for rejection of claims 4-7 and 2830 under 35 U.S.C. § 112, first paragraph, for failure to nicer the enablement requirement may be improper. Applicants thus respectfully request withdrawal of the rejections and reconsideration of these claims.

i. The Examiner respectfully replies:

ii. Regarding claims 5 and 9, the specification appears to require *all* of the digital outputs to be in a high impedance state, rather than *at least one*, as recited in the claims, in order for the analog circuit to provide the output signal at the node.

iii. The specification does not appear to teach how to make the invention wherein merely *at least one* of the digital outputs is in a high impedance state, and this factor is determinative because an ordinary artisan would not know how to make the claimed invention.

g. The Applicant argues:

h. The final Office action cites to Fig. 4 and its corresponding pp. 21-22 to support the basis for the enablement rejection of claims 5-7 and 9-12 under 35 U.S.C. § 1.12, first paragraph.

i. Applicants respectfully submit that "[l]imitations appearing in the specification but not recited in the claim should not be read into the claims." MPEP § 2106 citing E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1.369, 67 USPQ2d

1947, 1950 (Fed. Cir. 2003). Applicants respectfully submit that Fig. 4 and pp. 21-22 merely represent one or some embodiments of the invention and thus should not be read into the claims.

j. In addition, Applicants respectfully point to several examples in the Specification which provide clear written description to enable one of ordinary skill in the art to make and use the claimed invention without undue experimentation. Applicants further respectfully note that the following examples are provided for illustration and explanation purposes only.

k. Applicants first respectfully point to p. *3, 20-p. 4, 1. 6* which provides, as some background information and to the extent pertinent, that "the value 'Z', however, does not represent a state of either 0 or 1. The value 'Z' ... represents the state of a signal not being driven or floating...When not actively driving a signal, an electronic device...may present a high-impedance state, or 'Z' state, at its output.

l. Applicants then respectfully point top. *13,11, 10-16* which illustrate some embodiments of the claimed invention. These passages show that when an analog circuit block receives a Z value (i.e., **floating** value) of an input (i.e., the input is not being driven), simulator 100 enables the **analog** circuit block to **solve for that node** as if it were **an output of the analog** block_ *P. 19,1, 18-p. 29, 1. 7* further illustrates that, in some embodiments, when an input to analog block 203 is a Z value, then such an input to analog circuit block 203 is not being driven by another device or circuit. In this case, simulator 100 solves for the analog circuit block 203 absent the input to analog block 203 and propagates the analog block solution (i.e., signal value) to other fallouts of net 202 using **the output portion of the analog input.** These passages clearly provide sufficient written description to enable one of ordinary skill in the art to make and use the claimed invention as encompassed in claim 5 which, in part recites "simulating the circuit design by modeling at least one of said output . . **as an analog output** signal from said analog circuit to said node when said at least one of said output is **in said high impedance state"** (emphasis added.)

i. The Examiner respectfully replies:

ii. Regarding claims 5 and 9, the specification appears to require *all* of the digital outputs to be in a high impedance state, rather than *at least one*, as recited in the claims, in order for the analog circuit to provide the output signal at the node. The Applicant's arguments above appear to support the rejection because in order for the input to the analog block to be a Z value, all the digital outputs must be a Z value.

m. The Applicant argues:

n. In addition, Applicants respectfully point to p. 1.2, 1. 16–p. 13,1. 9 which states, to the extent pertinent, "when digital gate 201 drives any non-Z value onto network node 202, every fanout of net 202 including analog circuit block 203 connected to net 202 (analog block 203 in this example includes, among other things, components R1/1(2 and transistor devices MI/M2) receive this non-Z value as an input. However, when digital gate 201 is not driving an output signal of 0, 1, or X, digital gate 201 presents a Z value (i.e., floating) output onto net 202 .....That is, when the digital gate 201 drives any non-Z value (i.e., not floating or not in high impedance state), every fanout of net 202 including analog circuit block 203 receives **this non-Z value as an input rather than an output** as illustrated in the preceding paragraph immediately above when the di[9]ital circuit block is not driving any non-Z values. Applicants therefore respectfully submit that these exemplary paragraphs clearly provide sufficient written description for the claimed invention of the independent claim 5 which recites, to the extent pertinent, "simulating the circuit design by modeling at least one of said output as a **digital output** signal from the corresponding digital circuit to said node when said at least one of said output is not **in said high impedance state .. ."** (emphasis added.)

i. The Examiner respectfully replies:

ii. Regarding claims 5 and 9, the specification appears to require *all* of the digital outputs to be in a high impedance state, rather than *at least one*,

as recited in the claims, in order for the analog circuit to provide the output signal at the node. The Applicant's arguments above appear to support the rejection because when any digital gate drives a non-Z value, the non-Z value is used as the output rather than an analog value.

o. The Applicant argues:

p. Therefore, Applicants respectfully submit that since claim 9 recites similar limitations as does claim 5, and claims 6-7 and 10-12 depend from claims 5 and 9 respectively, claim 5-7 and. 9-12 are believed to have satisfied the requirements under 35 U.S.C. § 112, first paragraph. Applicants thus respectfully request the withdrawal of the rejections and reconsideration of these claims.

i. The Examiner respectfully replies:

ii. Regarding claim 9, since claim 9 is argued similar to claim 5, please refer to the replies for claim 5 above. Since the rejections of claims 5 and 9 are maintained, the rejections of the dependent claims are also maintained.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

a. **Claims 5 - 7 and 9 - 12** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. One reasonably skilled in the art

could not make or use the invention from the disclosure in the specification, coupled with information known in the art, without undue experimentation, for the following reasons:

i. Regarding independent claim 5 and dependent claims, claim 5 recites in the second limitation, "simulating the circuit design by modeling at least one of said output as a digital output signal from the corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one of said output is in said high impedance state". The specification appears to teach that all of the outputs of the plurality of digital circuits must be in a high impedance state in order for the analog output signal to be the final output (*refer to figure 4, and page 21, lines 11 – 22 through page 22, lines 1 – 11*). Further, the specification appears to teach that the plurality of outputs is resolved to a single value by the simulation, and that the single value is used to determine whether the final output is analog or digital. Further, the specification appears to teach that when the final output is analog, that a digital state value is also provided to any digital circuits using the output. Claim 6 also appears to recite that only "at least one of said output is in said high-impedance state" is needed for an analog output signal. Claim 7 appears to collectively resolve the digital circuit outputs into a single output signal, but does not appear to use the signal to determine whether an analog signal is output.

ii. Regarding independent claim 9 and dependent claims, claim 9 recites in the second limitation, "simulating the circuit by modeling at least one of said output provided by said one or more digital circuits as a

digital output signal from the corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said at least one of said output is in said high impedance state". The specification appears to teach that all of the outputs of the plurality of digital circuits must be in a high impedance state in order for the analog output signal to be the final output (*refer to figure 4, and page 21, lines 11 – 22 through page 22, lines 1 – 11*). Further, the specification appears to teach that the plurality of outputs is resolved to a single value by the simulation, and that the single value is used to determine whether the final output is analog or digital. Further, the specification appears to teach that when the final output is analog, that a digital state value is also provided to any digital circuits using the output. Claims 10 - 11 also appear to recite that only "at least one of said output is in said high-impedance state" is needed for an analog output signal. Claim 12 appears to collectively resolve the digital circuit outputs into a single output signal, but does not appear to use the signal to determine whether an analog signal is output.

iii. In the light of the discussion above, the following factors are determinative:

(1) The specification provides no guidance or essential details of how to make the invention where only at least one of the digital outputs is in a high impedance state, and the ordinary artisan would not know how to make the invention. Undue experimentation would be needed to make or use the invention based on the content of the disclosure.

(2) No evidence of a working example was provided which would indicate that even the Applicant was able to make the invention.

b. Weighing the evidence as a whole, the Examiner concludes that one reasonably skilled in the art could not make or use the invention from the disclosure in the specification, coupled with information known in the art, without undue experimentation, as discussed below.

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 17 - 18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

a. Regarding claims 17 – 18, a valid process under 35 USC § 101 must either 1) transform underlying subject matter, or 2) be tied to another statutory class, such as a particular apparatus. The claim does not appear to either transform underlying subject matter or be tied to another statutory class. In order to qualify as a statutory process, the claim should positively recite the other statutory class to which it is tied, for example by identifying the apparatus that accomplishes the method steps. A recitation of a computer in the preamble does not appear to be sufficient to tie the process to a particular apparatus. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88

USPQ 478, 481 (CCPA 1951). [I]t is assumed that the preamble language is duplicative of the language found in the body of the claims or merely provides context for the claims, absent any indication to the contrary in the claims, the specification or the prosecution history.

Allowable Subject Matter

9. Claims 1 – 20 are allowable over the prior art of record.

10. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

11. A reasons for indicating allowability of the claims was provided in previous Office Actions dated August 21, 2006 and March 21, 2006.

Conclusion

12. The following references made of record teach knowledge of the ordinary artisan:

a. David Overhauser et al., "Evaluating Mixed-Signal Simulators", 1995, IEEE 1995 Custom Integrated Circuits Conference, pages 113-120; teaches simulation of a bidirectional analog/digital node (*especially page 118, section IV. The Bidirectional Interface, and figures 14 and 15*).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Russ Guill whose telephone number is 571-272-7955. The examiner can normally be reached on Monday – Friday 9:30 AM – 6:00 PM.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Any

inquiry of a general nature or relating to the status of this application should be directed to the TC2100 Group Receptionist: 571-272-2100.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Russ Guill
Examiner
Art Unit 2123

RG

/Paul L Rodriguez/
Supervisory Patent Examiner,
Art Unit 2123